

## PEX 8311 Key Features

- ◆ Generic Local Bus to PCI Express Bridge
- ◆ Root Complex and EndPoint Modes of Operation
- ◆ Local Bus Modes:
  - 32-bit address & 32-bit data (C-Mode)
  - Multiplexed 32-bit address/data (J-Mode)
- ◆ Local Clock rates up to 66MHz
- ◆ Zero wait state bursts to 264MB/s
- ◆ Integrated SerDes
- ◆ 2 DMA channels
- ◆ 21mmx21mm, 337 pin PBGA
- ◆ Typical Power: under 1.0 Watt

## Other Features

- ◆ Integrated PCIe Interface
  - Compliant to PCIe r1.0a
  - x1 Link, 2.5 Gbps / Direction
  - Auto Polarity Reversal
  - Link CRC Support
  - Link / Device Power Management
  - Flow Control Buffering
- ◆ Direct Master Data Transfers
- ◆ Direct Slave Data Transfers
- ◆ Configuration Through Host or Optional EEPROM
- ◆ On-the-fly Endian Conversion
- ◆ 8 Mailbox & 2 Doorbell Registers
- ◆ Four GPIO, 1 GPI, 1 GPO
- ◆ I2O Messaging Unit

## Application:

### *Digital Video Surveillance System*

## PLX Product:

### *PEX 8311 – Local Bus to PCIe Bridge*

## Key Benefit:

### *Full Connectivity to PCIe components*

## New Security Systems Migrating to PCI Express Designs

Security systems have traditionally been extremely limited in their functionality and capabilities. Often, they simply detect open doors or windows and provide a basic warning on facility intrusions. Going forward, systems are routinely providing video surveillance cameras throughout an entire complex often with wireless feeds back to a central host. With numerous high resolution video feeds, comes an extensive increase in throughput and the need to use peer-to-peer switching of PCI Express standards, not the shared multi-drop legacy PCI bus. New frame grabber boards (see figure 1) take input from multiple feeds, process data locally, and feed this information to the central host motherboard for analysis and corrective action. PCIe is used to provide not only the bandwidth needed, but includes PCIe switches to aggregate these video feeds, and provides the PCIe connectivity.



Figure 1

## PEX 8311 Supports Full Protocol Translations

The PEX 8311 is a bridge from a low overhead parallel generic local bus, used by various processors, DSPs, memory, and FPGA designs, to a PCIe port. In this conversion, the bridge completely translates data from the local bus into PCIe packets with full packet header generation. Address spaces from the local bus and PCIe domain are fully translated. Out-of-band signals on the local bus are translated into message signaling interrupt (MSI) packets and vice versa. The bridge supports all transaction types. Full on-chip buffers provide flow control and the link layer CRC ensures data integrity.

## Multiple DMA Channels are Key

Figure 2 shows the PEX 8311 used on a frame grabber board. Here multiple digital cameras and other surveillance sources provide input to a JPEG device for compression and format conversion. Data is buffered through FIFOs before added processing in an FPGA. FPGA devices routinely use a local bus type interface and connect with no glue logic to the PEX 8311 bridge. The bridge converts traffic to PCIe and is aggregated through a PCIe switch, such as the PEX 8524 and then directed upstream to the motherboard. As there are multiple streams of data, several bridges are used in the design. A local CPU is used to manage this traffic flow. Memory or other components may also be present on this local bus.

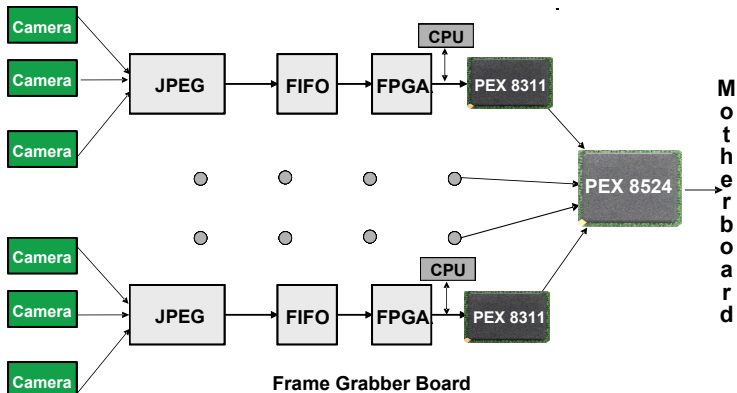


Figure 2

In order to more efficiently transfer data through this board, it is preferable to have multiple DMA channels present. The DMA controllers take a set of instructions from the local CPU or Host and control the transfer of data through the bridge negating the need for host intervention. With two DMA channels present, it simplifies the design as one set of descriptors can be loaded into one DMA channel while the second channel transfers data. In the limit of small packet size, throughput can be increased by 30%. A second use of multiple DMA channels is to allow simultaneous bi-directional traffic, control data, in this case, from the host back to the source. No need exists to complete one transfer before starting the second.

## Additional PEX 8311 Capabilities

Such applications often require large numbers of devices present on the local bus and have high bandwidth needs. Local bus devices need to communicate with each other and not just through the bridge. The PEX 8311 has the capability to handle up to five simultaneous loads present on the local bus with up to 32-bit and 66 MHz operation.

In addition, the PEX 8311 includes Direct Master and Direct Slave operation simultaneously with DMA. As these modes have higher priority than DMA, they can be used to provide control data or other throughput that cannot be blocked by DMA transfers. To enhance throughput even more, Read Ahead mode allows data to be obtained and stored in internal FIFOs before it is sent through the bridge.

## Design Tools & Documentation:

On PLX Public ToolBox:

[http://www.plxtech.com/products/pci\\_express/PEX8311/default.asp](http://www.plxtech.com/products/pci_express/PEX8311/default.asp)

- ◆ Data Book, Reference Design Kit, BSDL and HSPICE Models, Product Brief, Design Note

### Contact Information

PLX Technology, Inc.  
 870 Maude Ave.  
 Sunnyvale, CA 94085 USA  
 Tel: 1-800-759-3735  
 Tel: 1-408-774-9060  
 Fax: 1-408-774-2169  
 Applications Support: Local FAE  
 Product Marketing:  
 John Gudmundson  
[jgudmundson@plxtech.com](mailto:jgudmundson@plxtech.com)  
 Web Site: [www.plxtech.com](http://www.plxtech.com)

© 2006 PLX Technology, Inc. All rights reserved. PLX and the PLX logo are registered trademarks of PLX Technology, Inc. ExpressLane, PowerDrive and the PowerDrive logo are trademarks of PLX Technology, Inc., which may be registered in some jurisdiction. All other product names that appear in this material are for identification purposes only and are acknowledged to be trademarks or registered trademarks of their respective companies. Information supplied by PLX is believed to be accurate and reliable, but PLX Technology, Inc. assumes no responsibility for any errors that may appear in this material. PLX Technology, Inc. reserves the right, without notice, to make changes in product design or specification.

8311-SIL-EA-1.0