

### PEX 8648 Highlights

- 48-lane, 12-port PCIe Gen 2 Switch
- Compliant to the PCIe base spec r2.0
- Integrated Non-Transparent port
- 2KB maximum payload size
- Microsoft Vista compliant
- *performancePAK*<sup>™</sup> features
  - Full line rate on all ports
  - Non-blocking switch fabric
  - Read Pacing<sup>™</sup>
  - Dual Cast<sup>™</sup>
  - Dynamic Buffer Allocation
- *visionPAK*<sup>™</sup> features
  - SerDes eye-width capture
  - Per port performance monitoring
  - Error injection and loopback
  - PCIe Packet Generator
- 140ns max packet latency (x16 to x16)
- Per port error diagnostics
- Advanced error reporting
- Port status bits and GPIO pins
- INTA# and FATAL\_ERR# signals
- Memory (RAM) error correction
- Data path parity
- ECRC and Poison bit support
- 3 Hot-Plug ports with native Hot-Plug signals
- All ports Hot-Plug capable thru I<sup>2</sup>C

### Application:

## **Server and Storage Systems**

### PLX Product:

## **PEX 8648 – 48-lane, 12-port PCIe Gen 2 Switch**

### Key Benefit:

## **Industry's Only x16 port and *visionPAK*<sup>™</sup> Toolkit**

### Building new PCIe Gen 2 Systems

The new generation of server and storage systems will implement PCIe 2.0 to take advantage of the increased bandwidth offered by PCIe Gen 2 based chipsets and processors. Currently, most RISC CPUs and all new server/storage chipsets for x86 CPUs offer PCIe Gen 2 interfaces. RISC CPUs are available with x4 and x8 ports, while chipsets for x86 CPUs offer up to 36 PCIe Gen 2 ports. The chipset's PCIe ports can be configured as x1, x4, x8 or x16.

High-end graphics systems use x16 to connect to GPUs today and it is expected that new server and storage systems will utilize x16 capabilities as well. This will allow end-user applications to maximize the utilization of resources (hardware) and increase the throughput of the system. In order to take advantage of the x16 port of the chipset, users must design their systems using the switches that support x16 ports, thus allowing fan-out of x16 port of the chipset to multiple narrower ports (such as x8, x4) for aggregation.

Another advantage of a x16 port is that it allows designers to aggregate high bandwidth end-points such as 10GE NICs or 8G FC-HBAs without creating a bottleneck at the port connected to the host.

PCIe Gen 2 has a signaling rate of 5GHz/s, which is still new for server and storage system designers. This high speed signaling creates many challenges for designers in the form of signal integrity, error rates, flow control, board debug and system debug. Hardware designers must select components that not only offer ease of device debug but also provide assistance in system level debug.

### **PEX 8648 supports x16 ports & debug features**

PLX recognized the need for x16 PCIe ports and debug features early on and included them in their PCIe Gen 1 switches. When PCIe Gen 2 was introduced, PLX continued the support for x16 ports and enhanced the switch's system and chip debug capabilities by introducing the *visionPAK* toolkit.

PLX is the only PCIe switch company that supports x16 link-widths. Currently, PLX supports a x16 port configuration in its 96-, 80-, 64-, 48-, and 32-lane PCIe Gen 2 switches. Although this document focuses on PEX 8648, most of the features, capabilities, and benefits discussed here also apply to all other PLX PCIe Gen 2 switches.

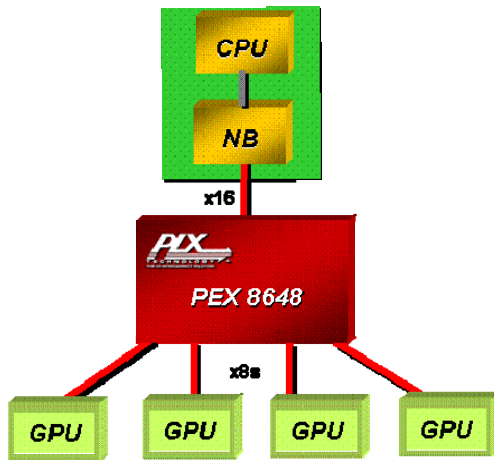


Figure 1. PEX 8648 in quad GPU application

Figure 1 above shows a quad-GPU application where the PEX 8648 is being used to provide a high-bandwidth link between four general purpose GPUs and the host CPU in a high-performance compute-server application. PEX 8648 also supports “true” peer-to-peer communication which allows the GPUs to exchange traffic without the need of CPU support for enhanced performance.

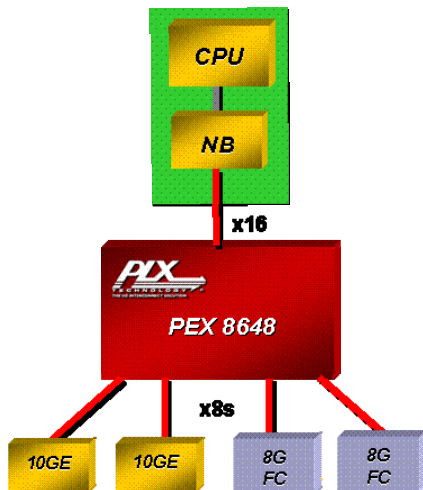


Figure 2. PEX 8648 in server application

Figure 2 illustrates the use of the PEX 8648 in server applications where high speed storage and communication I/Os are connected to the host via the switch.

The *visionPAK* toolkit for PEX 8648 is a combination of features designed and integrated in the silicon and software developed to allow for ease of use. The *visionPAK*, through a user friendly interface, enables the following:

- Access and measurement of Rx eye on internal pads
- Error injection in the data path to see system behaviors
- Packet generation to saturate up to x16 wide Gen 2 port
- Monitor errors, link utilization and performance
- PRBS and loop-back at various stages of data path
- Access to internal parallel data path and state-machines
- View of the PCIe hierarchy of the system

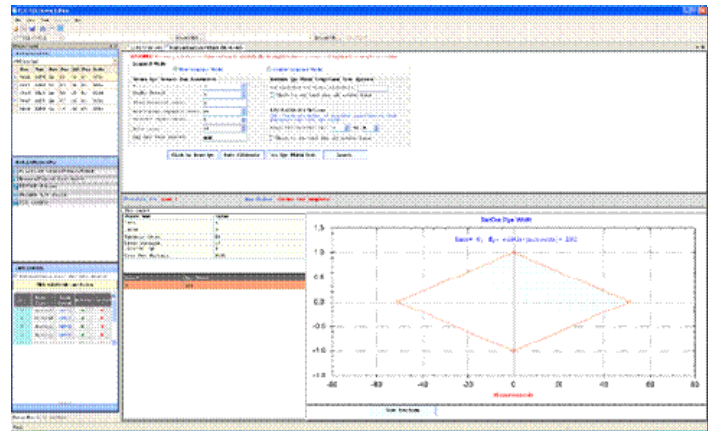


Figure 3. *visionPAK* software GUI

### Additional PLX Advantages

In addition to the above key features such as x16 link-width support and enhanced debug and system bring-up features, PLX switches support non-transparent bridging for host isolation, dynamic buffer/credit allocation for enhanced performance, and advanced power management techniques for power sensitive applications.

Additionally, following features are also supported:

- Any port can be programmed as the upstream port
- Advanced error reporting
- Per port error diagnostics

### Available on PLX Website:

Product Brief, Databook, Application Notes, technical support <http://www.plxtech.com/8648>