

## PEX 8664 Highlights

- 64-lane, 16-port PCIe Gen 2 Switch
- Compliant to the PCIe base spec revision 2.0
- Supports up to 5 upstream/host ports with 1+1 or N+1 failover to other upstream ports
- Supports PCI-SIG defined Multicast
- Integrated Non-Transparent port
- 2KB maximum payload size
- Microsoft Vista compliant
- *performancePAK* features
  - Full line rate on all ports
  - Non-blocking switch fabric
- *visionPAK* features
  - Serdes eye capture
  - per port performance monitoring
  - error injection and loopback
- 176ns max packet latency (x16 to x16)
- Per port error diagnostics
- Advanced error reporting
- Port status bits and GPIO
- INTA# and FATAL\_ERR# signals
- Memory (RAM) error correction
- Data path parity
- ECRC and Poison bit support
- 4 Hot-Plug ports with native HP signals
- All ports Hot-Plug capable thru I<sup>2</sup>C

### Application:

## ***Using Multicast in PCIe systems***

### PLX Product:

## ***PEX 8664 – 64-lane, 16-port PCIe Gen 2 Switch***

### Key Benefit:

## ***Multicast, and up to 5 upstream ports, provide efficient CPU utilization and failover***

### About Multicast

Traditional PCIe systems have relied only on unicast packets. This made sense since there was only one host at a given time and most of the communication was host-centric, i.e. the host communicated with all the endpoints one-at-a-time. Few applications had peer-to-peer communication but this communication was also routed through the host due to limitations in some vendors PCIe switches.

However lately, there have been more systems that use multiple hosts and have multiple end points that need to communicate at the same time. Also, as PCIe technology is being used in telecommunications and embedded (along with Graphics, Server and Storage) markets, the need for communication with more than one endpoint grew. This is where multicast comes in handy.

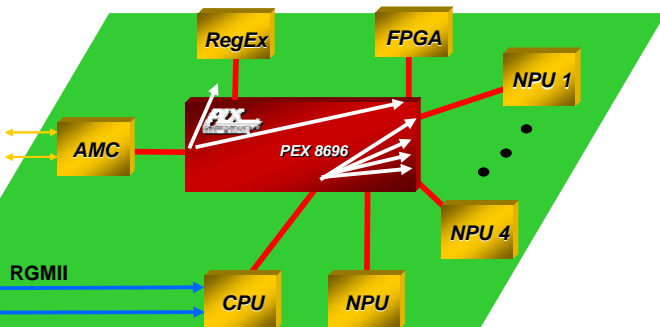
The multicast feature allows each host to communicate to all the endpoints at the same time. This eliminates the need for the host to write a unicast packet multiple times to each of the endpoints. Multicast improves the efficiency of the processor enabling it to focus on computational tasks and add value to the system. The following looks at some of the multicast usage models in the major markets and the advantages it brings to system designers.

### PLX Devices Supporting Multicast

PEX 8696 – 96 lanes and 24 ports with 8 upstream ports,  
PEX 8680 – 80 lanes and 20 ports with 6 upstream ports,  
PEX 8664 – 64 lanes and 16 ports with 5 upstream ports and  
PEX 8649 – 48 lanes and 12 ports with 4 upstream ports

\*\* The above four Gen 2 PCIe switches support multicast

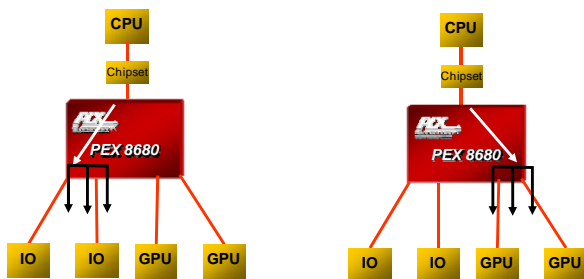
Figure 1 shows a usage model for multicast using PEX8696. In this figure, the AMC is able to multicast to two ports simultaneously while the CPU is able to multicast to four ports. Such a usage model ensures that each CPU performance is being maximized by issuing a packet only once instead of sending the same packet multiple times.



**Figure 1. PEX 8696 using multi-cast to enable communication between multiple end-points for efficient CPU utilization**

The other unique feature offered in PEX 8696 is the support for a x16 wide port. PLX is the only vendor to offer this support in PCIe switches.

Figure 2 shows a usage model for multicast using PEX 8680 and highlights the usage of multicast groups.

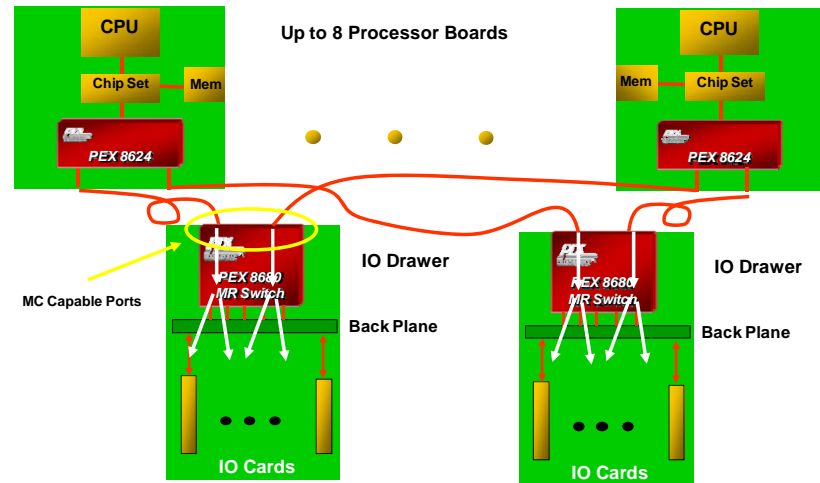


**Figure 2. Multicast groups using PEX 8680**

In figure 2 on the left diagram, the CPU is sending a single command to multiple I/Os (group 1) and the in the figure on the right, the CPU is sending command to multiple GPUs (group 2). This usage model shows the ability to group different end points into different groups so that a packet

can be sent to multiple endpoints in the same group. Up to 64 such groups are possible.

Figure 3 shows multicast in a storage environment. In this usage model a PEX 8680 device is used on the IO Drawers to multicast packets coming in from a processor board.



**Figure 3. Multicast in a storage application**

All four devices mentioned here provide end-to-end CRC (ECRC) protection and Poison bit support to enable designs that require end-to-end data integrity. It also supports data path parity and memory (RAM) error correction circuitry throughout the internal data paths as packets pass through the switch.

### Additional PLX Advantages

In addition to the above key features in these four devices such as multiple upstream ports, multicast, x16 support, integrated NT port, there are additional features implemented in these devices that are extremely useful in customer applications:

- Moveable upstream port – any port can be re-assigned as the upstream port
- Read Pacing for fair bandwidth allocation
- Advanced error reporting
- Per port error diagnostics
- Dynamic buffer/FC credit pool

### Available on PLX Website:

Product Brief, Databook, Application Notes, technical support  
<http://www.plxtech.com/8664>